Jitter Measurements over WorldFIP

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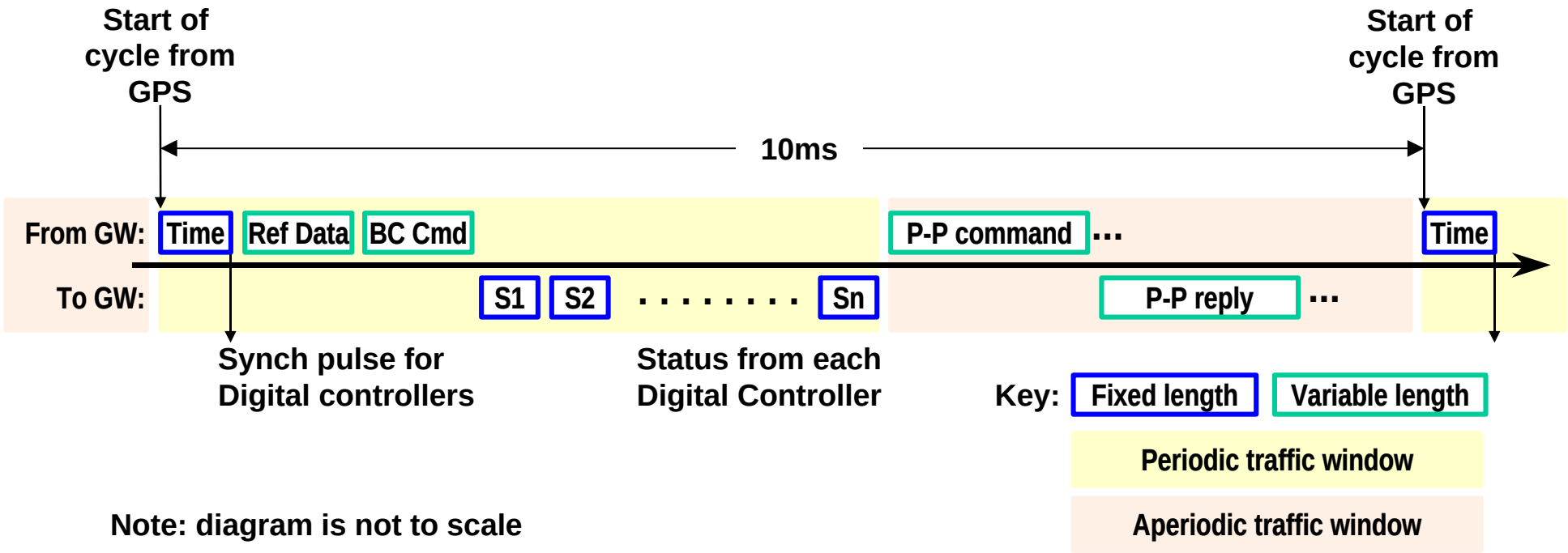
Traffic over the WorldFIP Fieldbus

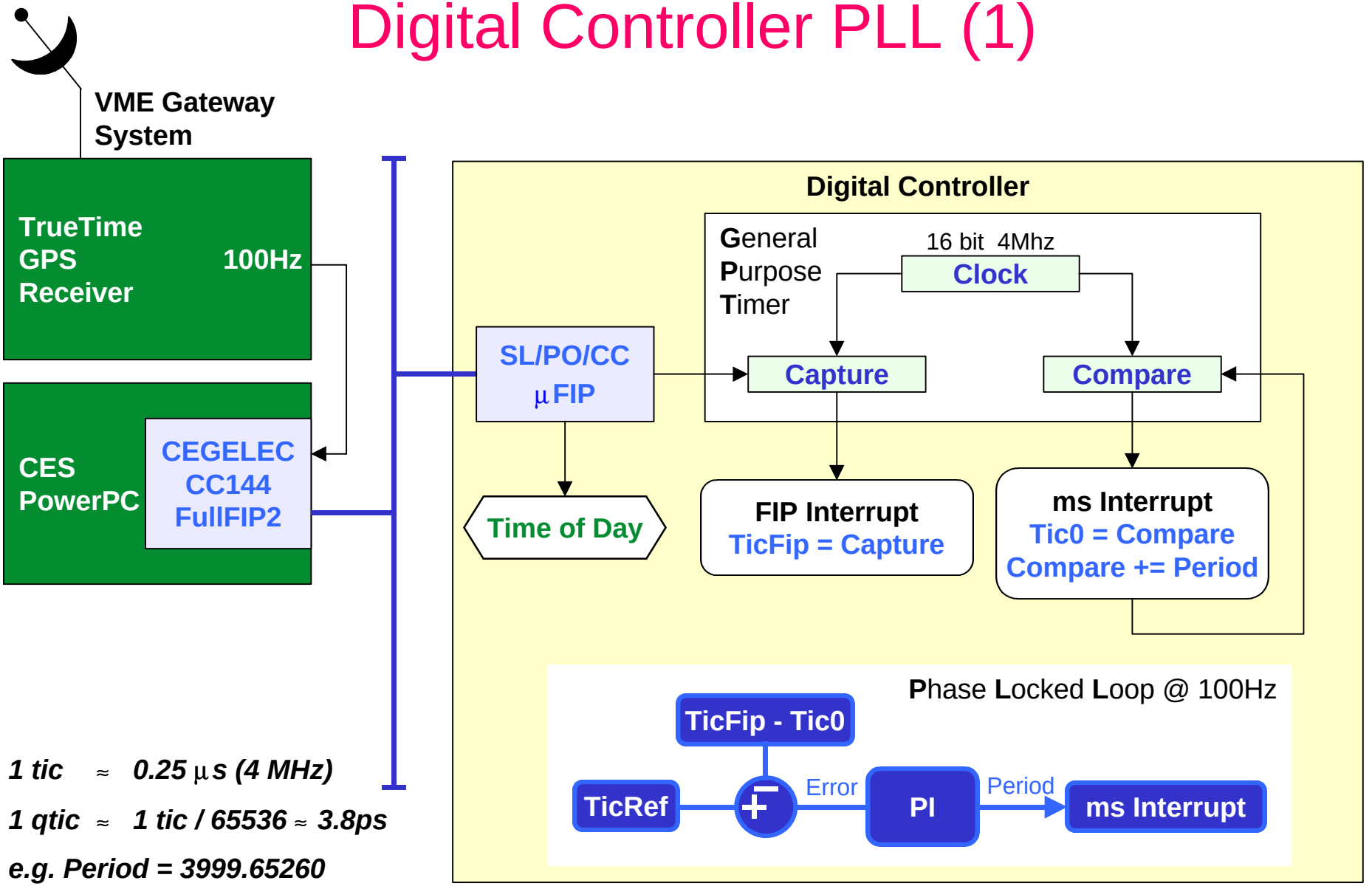
Fieldbus Cycle Structure

The Gateway is the Bus Arbitrator for the Fieldbus. It has a table defining the order of transmissions for each cycle. The cycle time has been chosen to be 10ms.



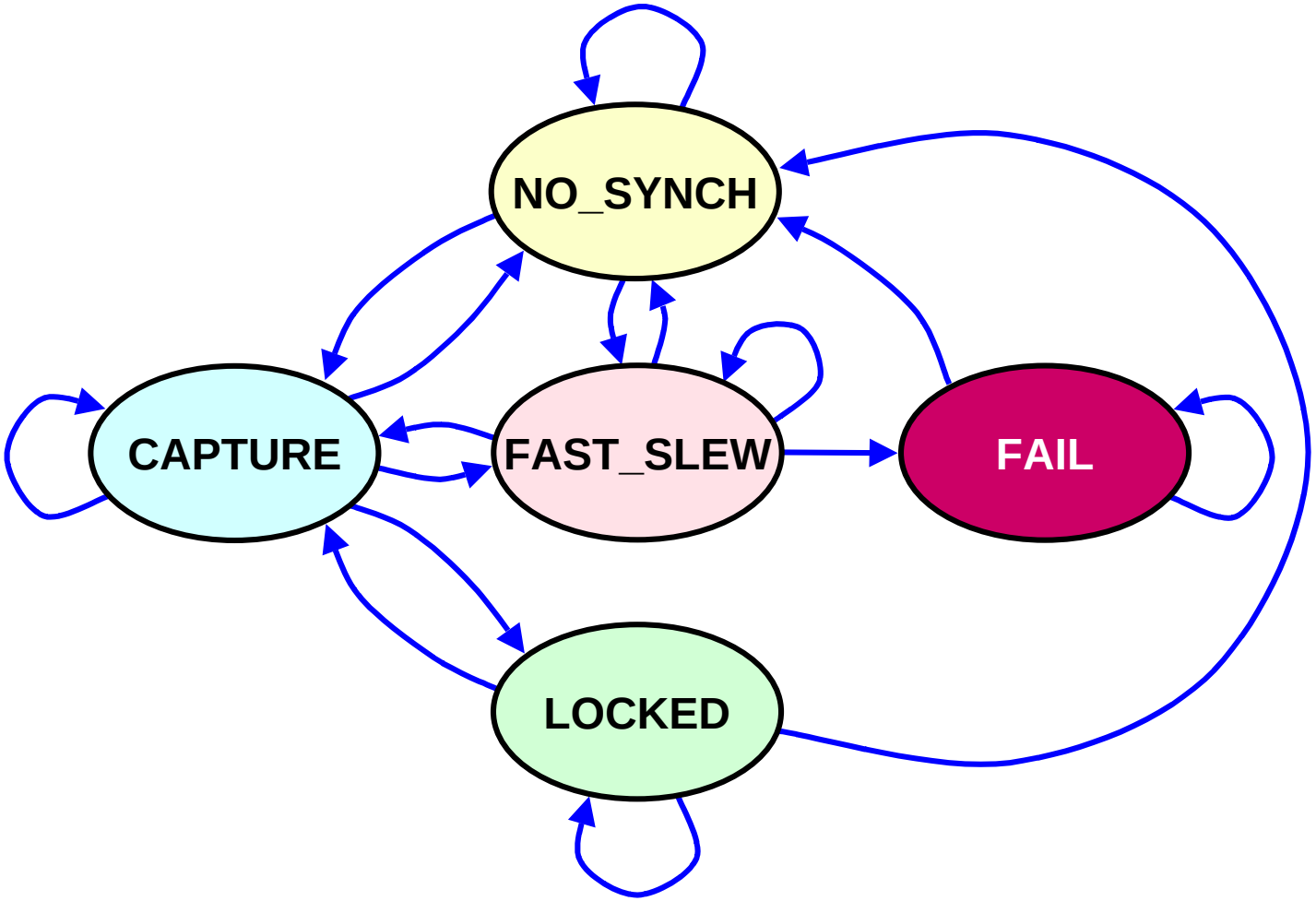
Note: diagram is not to scale

Digital Controller PLL (1)

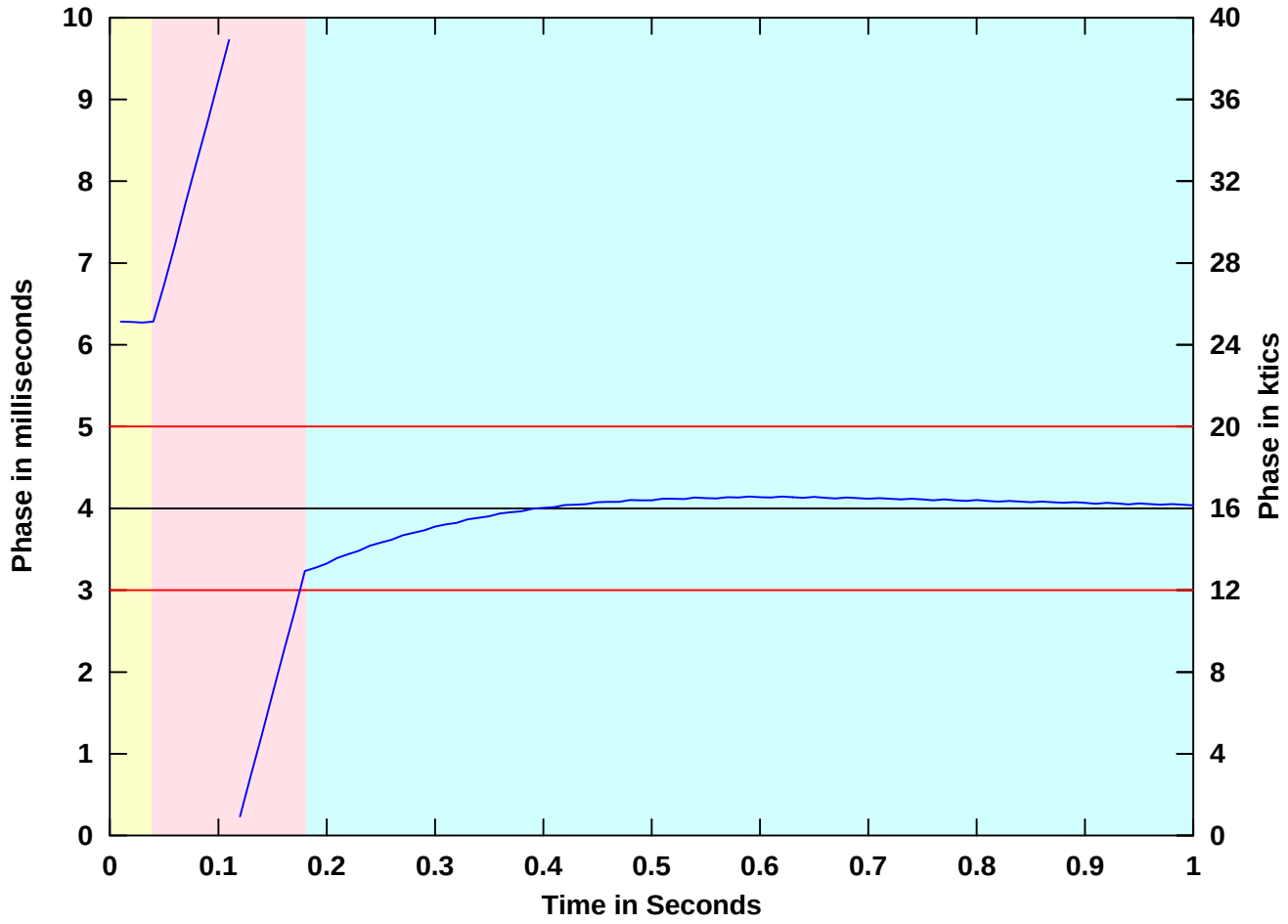


Digital Controller PLL (3)

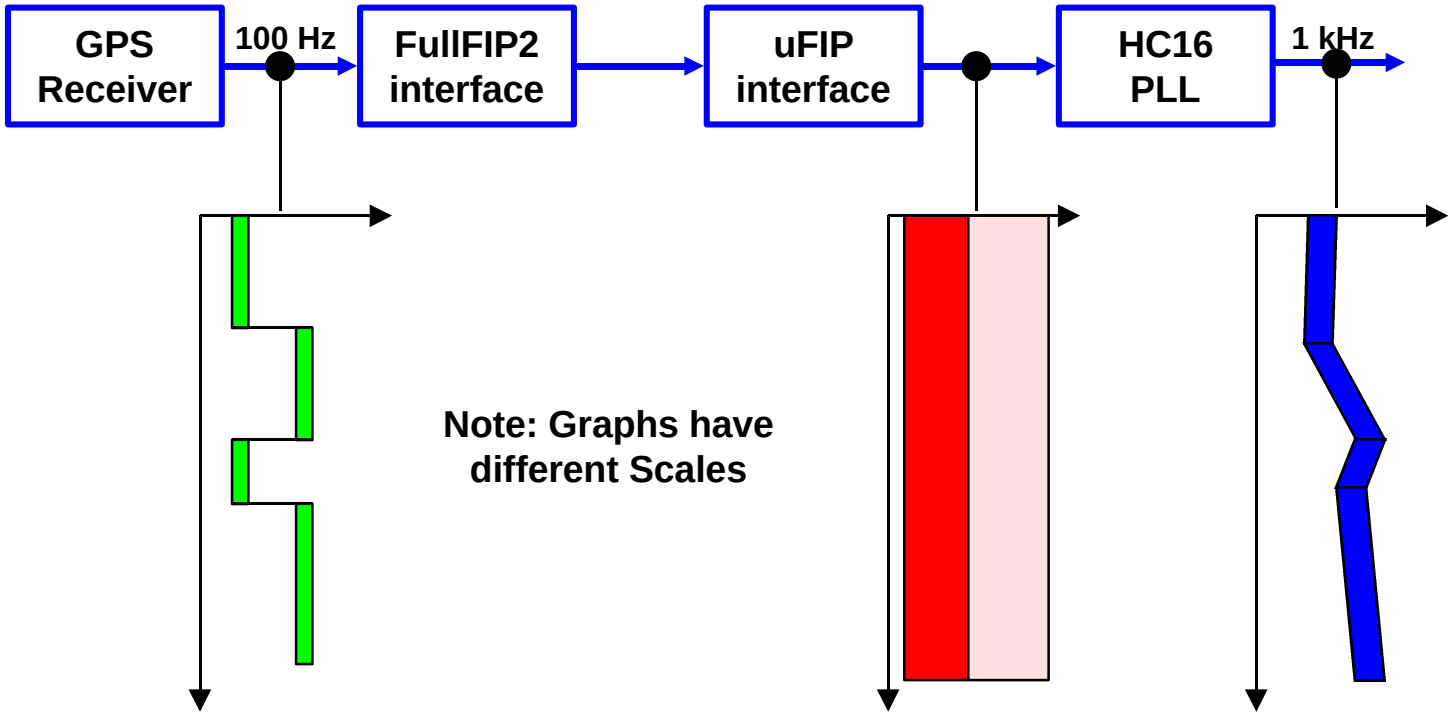
State Machine for Digital Controller Phase Locked Loop



Digital Controller PLL (2)



Synchronisation Over WorldFIP



Base jitter: 100 ns

Jump jitter: 400 ns

Base jitter: 3.5 μs

Max jitter: 7.2 μ s

Base jitter: 400 ns

Max jitter: 1.3 μs

PLL Frequency error: < 0.1 ppm (1ms after 2.5 hours)

Summary

- **Highly precise distribution of synchronised time over WorldFIP has been successfully demonstrated.**
- **Start of a ramp at a specified time has been demonstrated.**
- **Overall event distribution method is still to be decided.**
- **Digital Controller Hardware design needs to be frozen within 1 year, so a decision on event distribution (at least as far as it affects the bottom layer) is needed soon.**