TIMING WORKING GROUP

SL/PO Group Requirements For LHC

J. G. Pett

Proposed Infrastructure

All Power Converters (~ 1800) will be located either

- In the old LEP klystron galleries at each even point
- Or in the tunnel underneath the cryostat of the machine
- Plus a few elsewhere, including Experiments

Communications will be via WorldFIP field bus only, ie. no timing cable and Rx's

- Each bus will support a max of 30 power converters
- Each bus will be driven from a gateway computer PowerPC + LynxOS
- Each gateway will have a TG8* + GPS Timing modules

Proposed Operation

The Cern-wide TIMING will

- Provide the 10 ms ticks for global synchronisation of the WFIP frames, via TG8+GPS
- Each Power Converter Digital Controller will lock on to the 10 ms and produce 1 ms synch. pulses
- Timing "events" will be sent, as usual, to the TG8 as WARNING events (implicit fixed delay of ~100 ms)
- PowerPC then sends 'do this at absolute time T', to all "enabled" Digital Controllers
- No restrictions on number of "events", but total expected is small (ie. < 10, major one is 'start ramp').

Generalities

There is a need to define calendar/timestamp data format(s).
None of the above structure has yet been tested, but will be shortly.
The above process saves the timing cards and cabling but also allows for feedback thus avoiding 'most' errors due to false starts, missing ms etc.