Transmitting Timing over the WorldFIP fieldbus

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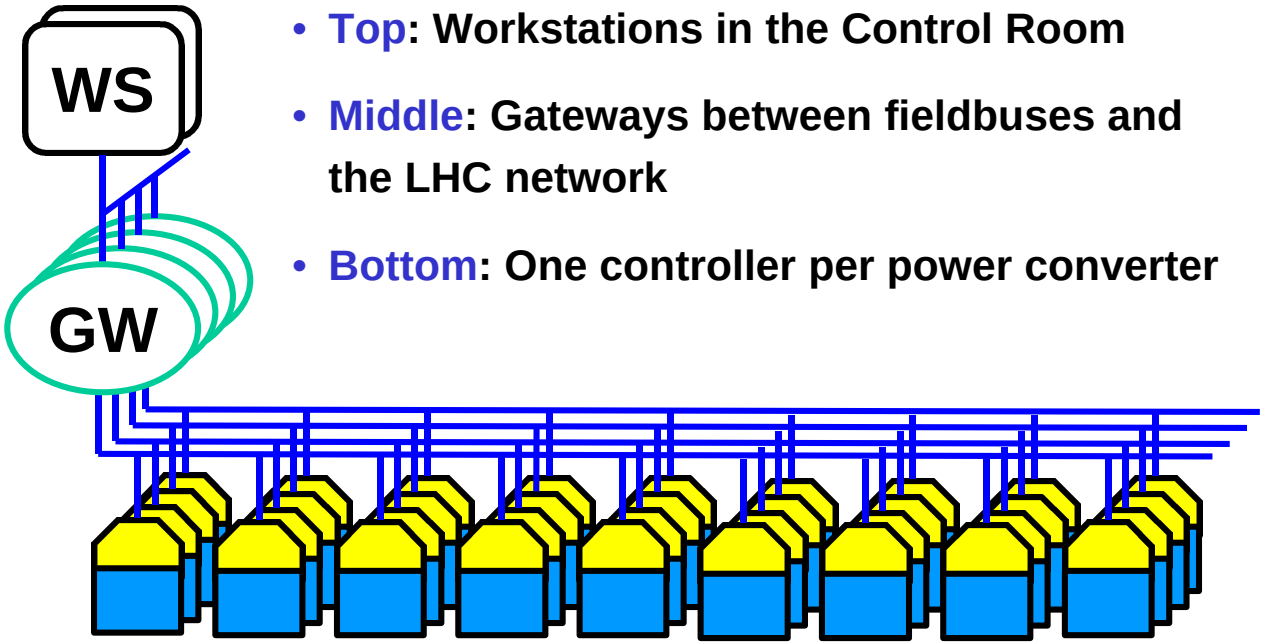
Project Objectives

- **Use the WorldFIP fieldbus to synchronize the clocks on all LHC Power Converter Controllers to better than 1 ms, compared to an absolute standard.**
- **Maintain this synchronization for up to 1000s without communication.**
- **Support “events” based on absolute time.**

System Architecture

String	LHC
A few	Quite a few
1	~100
~ 25	~ 1800



Three layer system, similar to LEP:

- **Top: Workstations in the Control Room**
- **Middle: Gateways between fieldbuses and the LHC network**
- **Bottom: One controller per power converter**

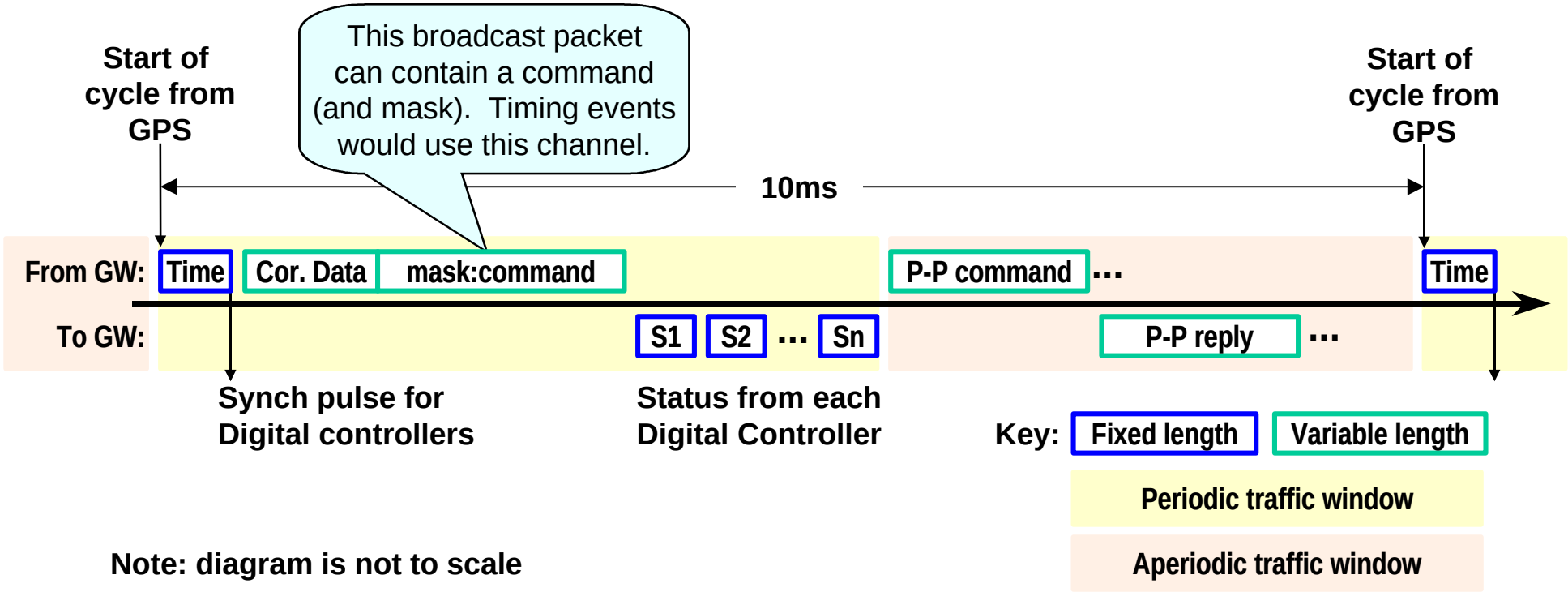
WorldFIP Fieldbus Characteristics

The WorldFIP fieldbus has been selected for the link between the gateways and the digital controllers. It's main features are:

- **2.5Mb/s over shielded twisted pair.**
- **Up to 32 nodes per bus without repeaters (256 with repeaters).**
- **500m length with the best quality cable.**
- **Deterministic traffic under the control of a Bus Arbitrator node.**
- **Low cost interface for Digital Controller nodes (cannot be Bus Arbitrator).**
- **Broadcast of synchronized timing is possible (jitter <20us).**
- **Fixed length and variable length (1-128 bytes) packets.**
- **Broadcast and point-to-point addressing.**
- **Periodic and aperiodic transmission.**

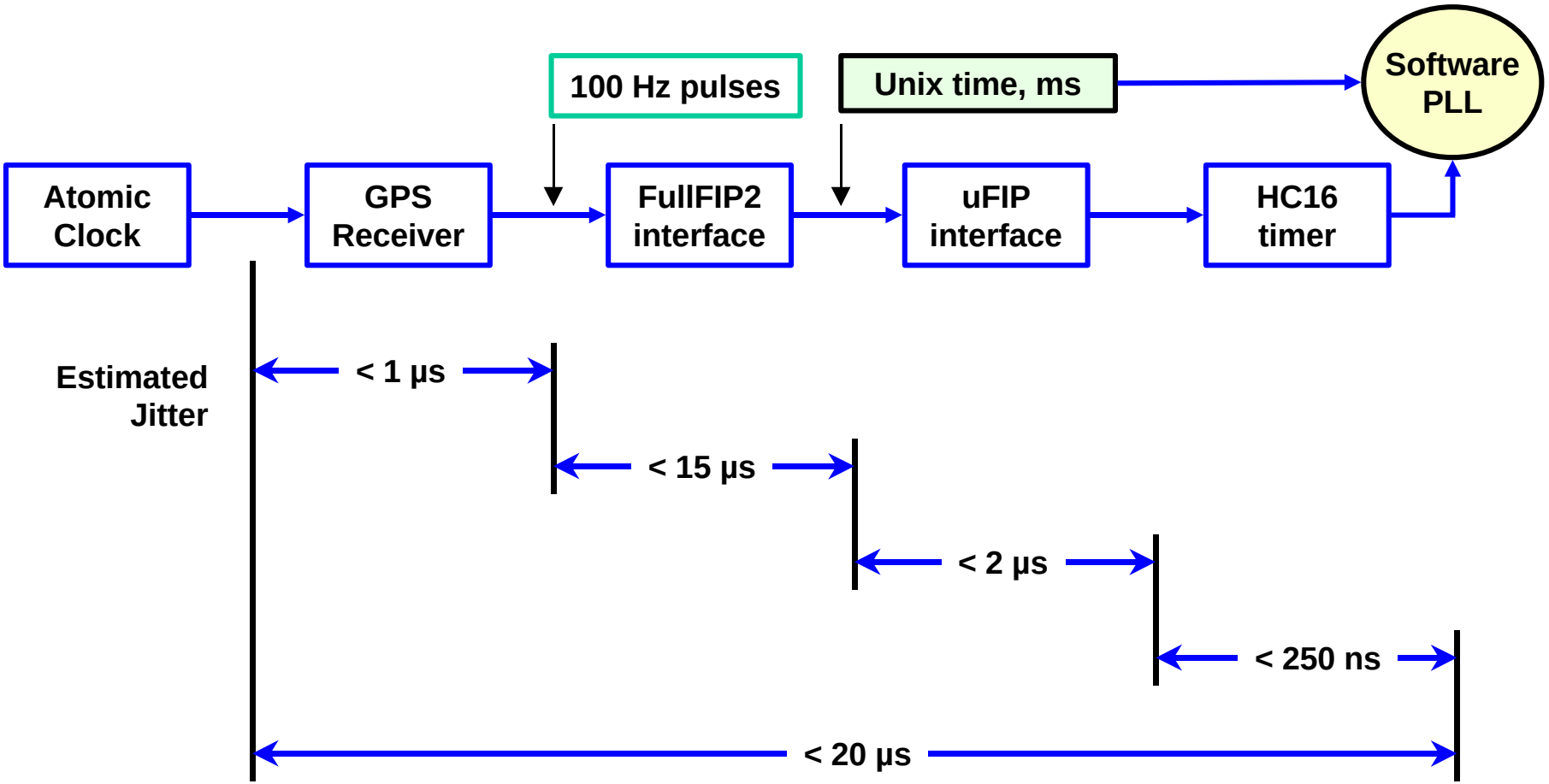
WorldFIP Fieldbus Traffic

The Gateway is the Bus Arbitrator for the Fieldbus. It has a table defining the order of transmissions for each cycle. The cycle time has been chosen to be 10ms, to allow 100Hz distribution of correction data and collection of status.



Note: diagram is not to scale

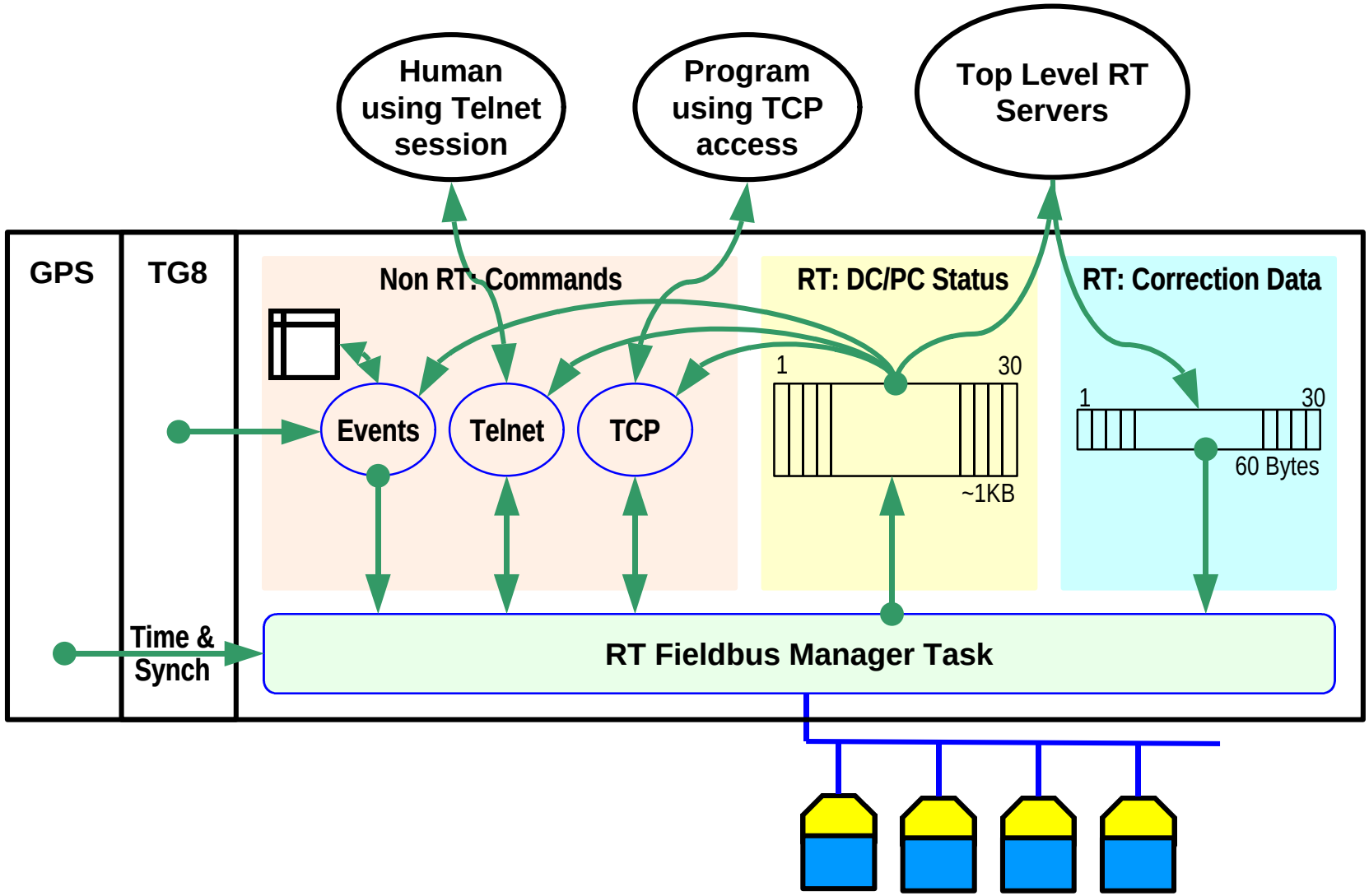
Synchronization Chain



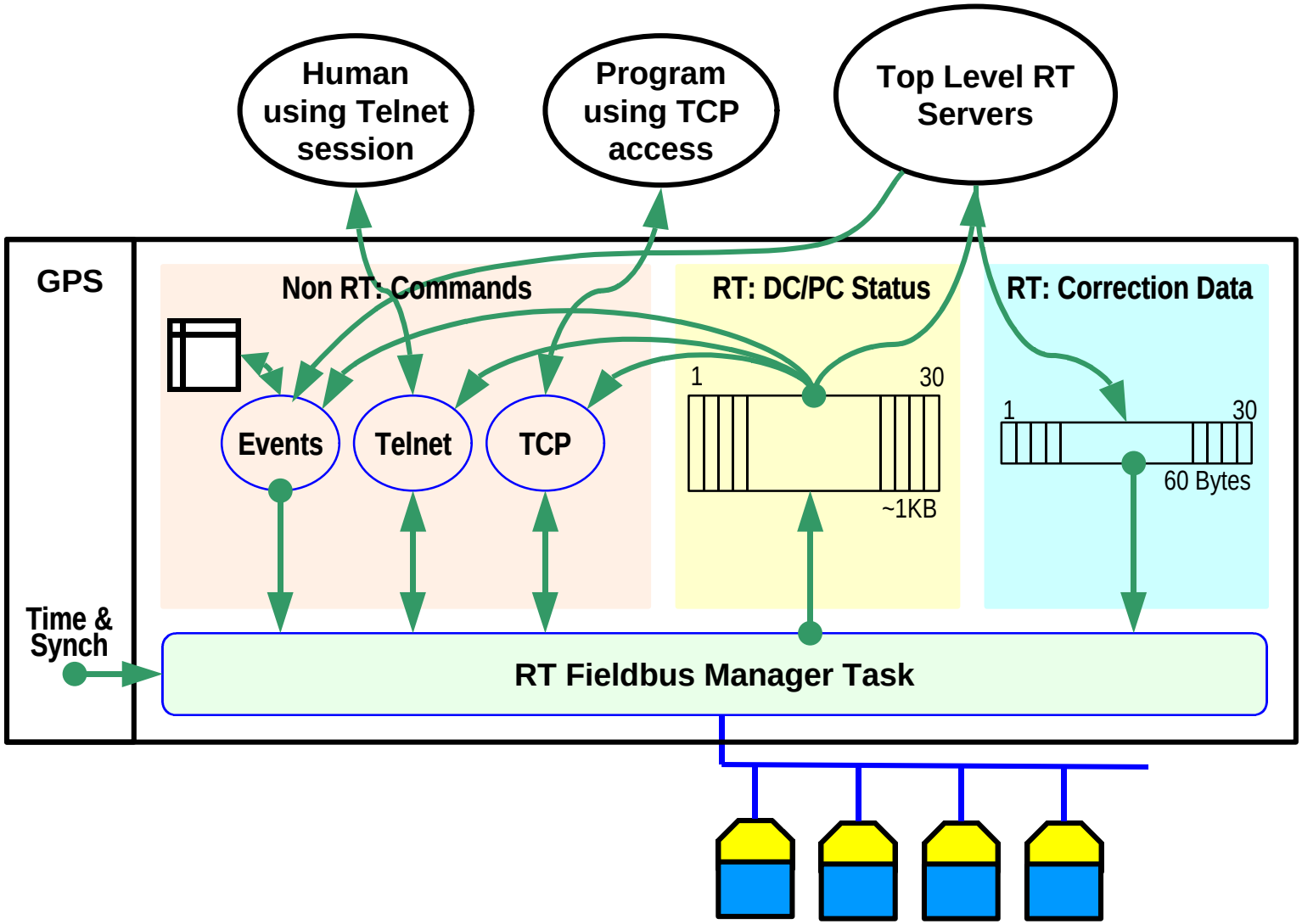
Software Phase Locked Loop

- Uses 100 Hz, 20µs jittered pulses from MicroFIP interface to generate 1 kHz, 1 µs jittered pulses from HC16 timer.
- Average frequency of HC16 timer is smoothly variable.
- In the event of loss of communication, the HC16 average 1 kHz clock period will be within 0.5 ppm of the external clock (1 ms error in 2000 s).
- Capture time is 2 s.
- Full equilibrium takes 30 s.
- Robust.

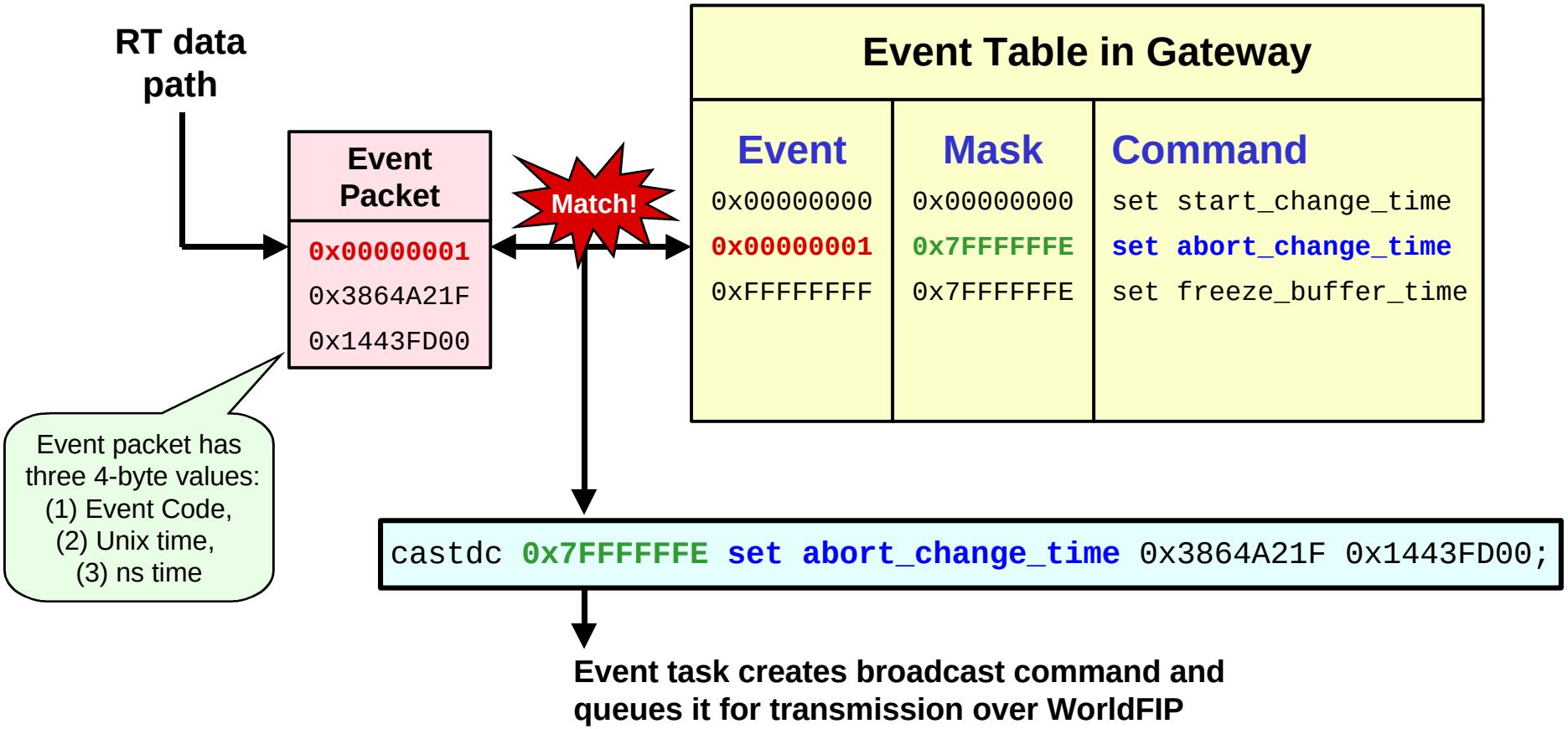
Gateway Architecture using TG8



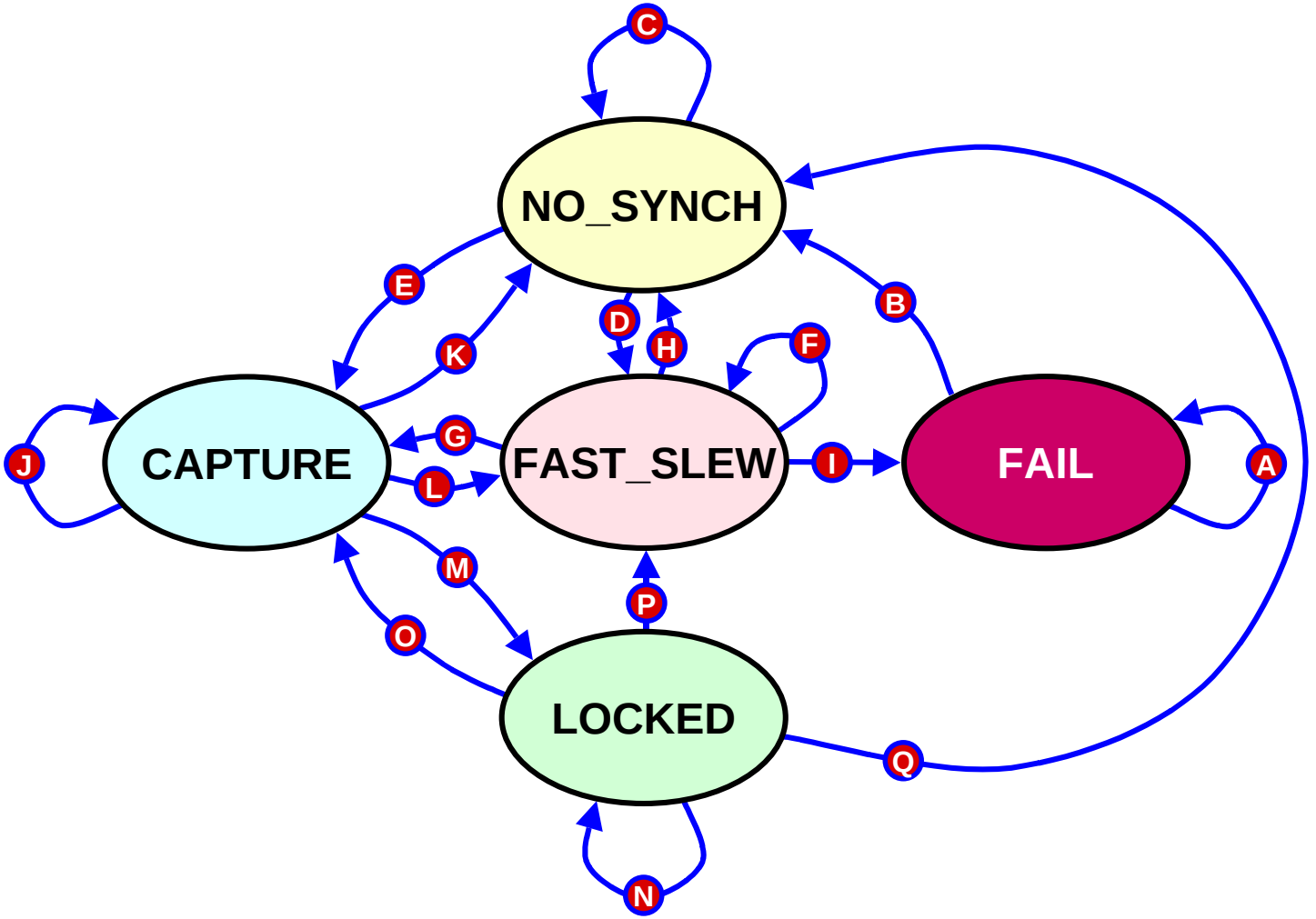
Gateway Architecture without TG8



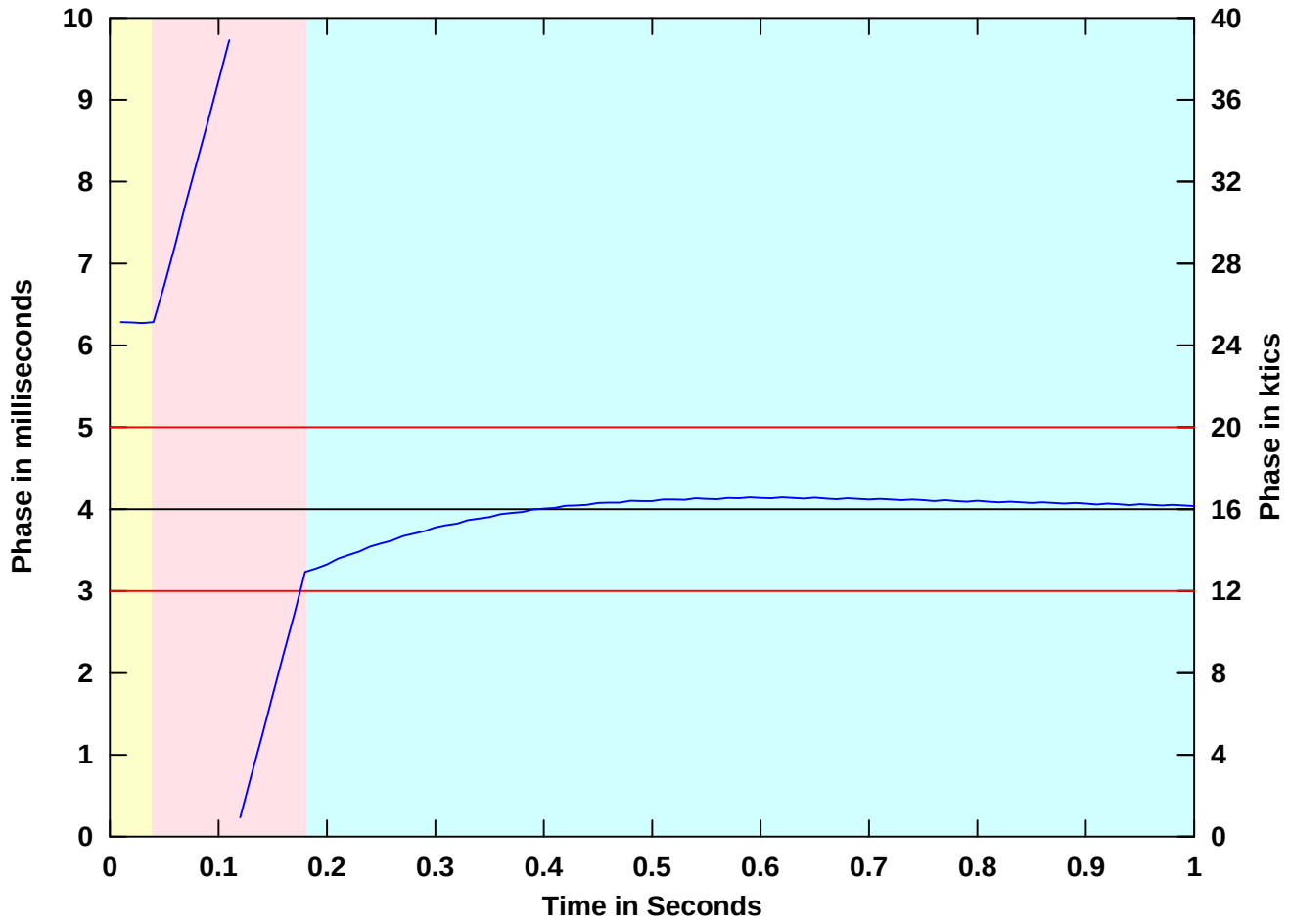
Possible Operation of Absolute Time Events



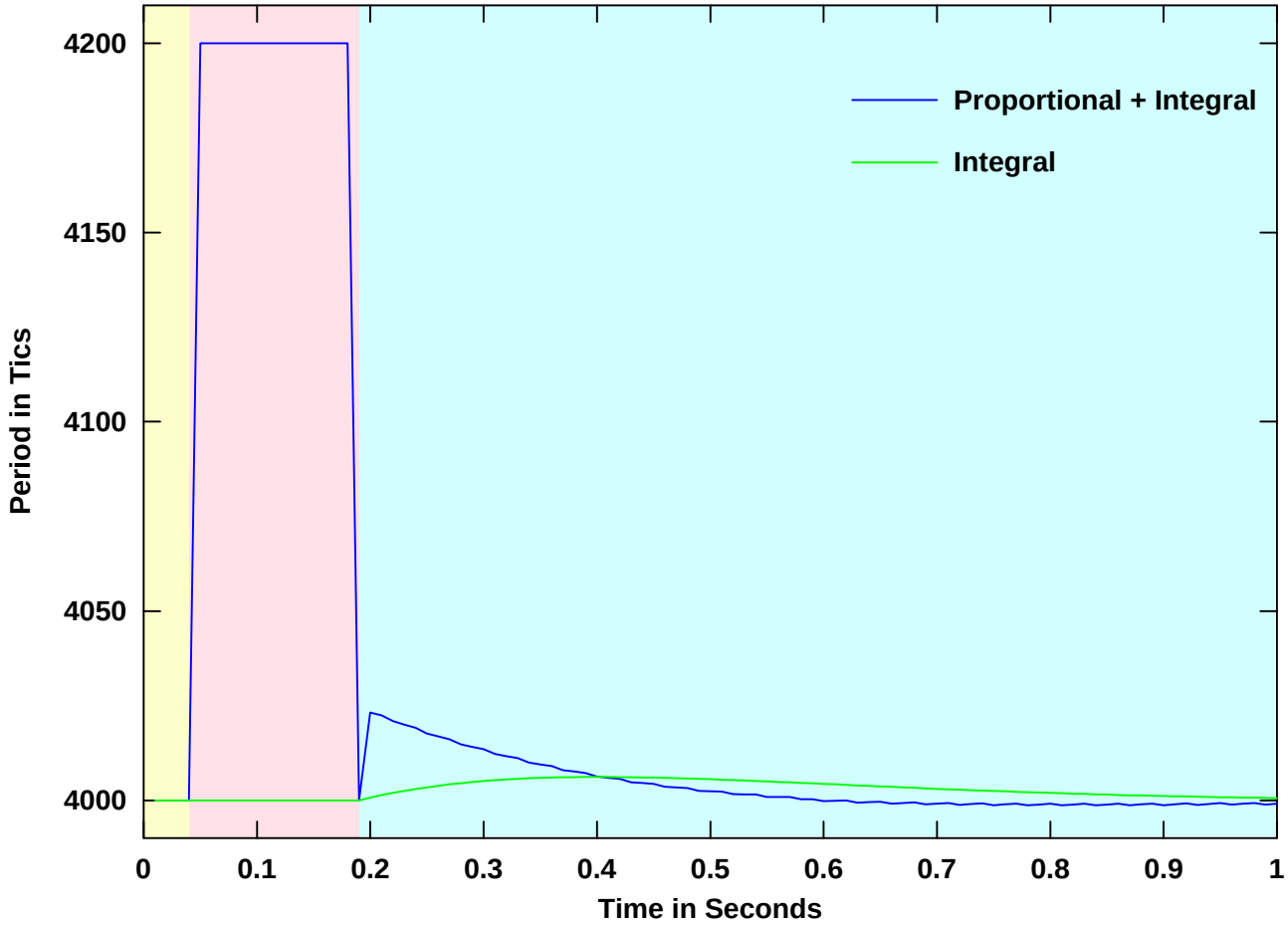
Phase Locked Loop State Machine



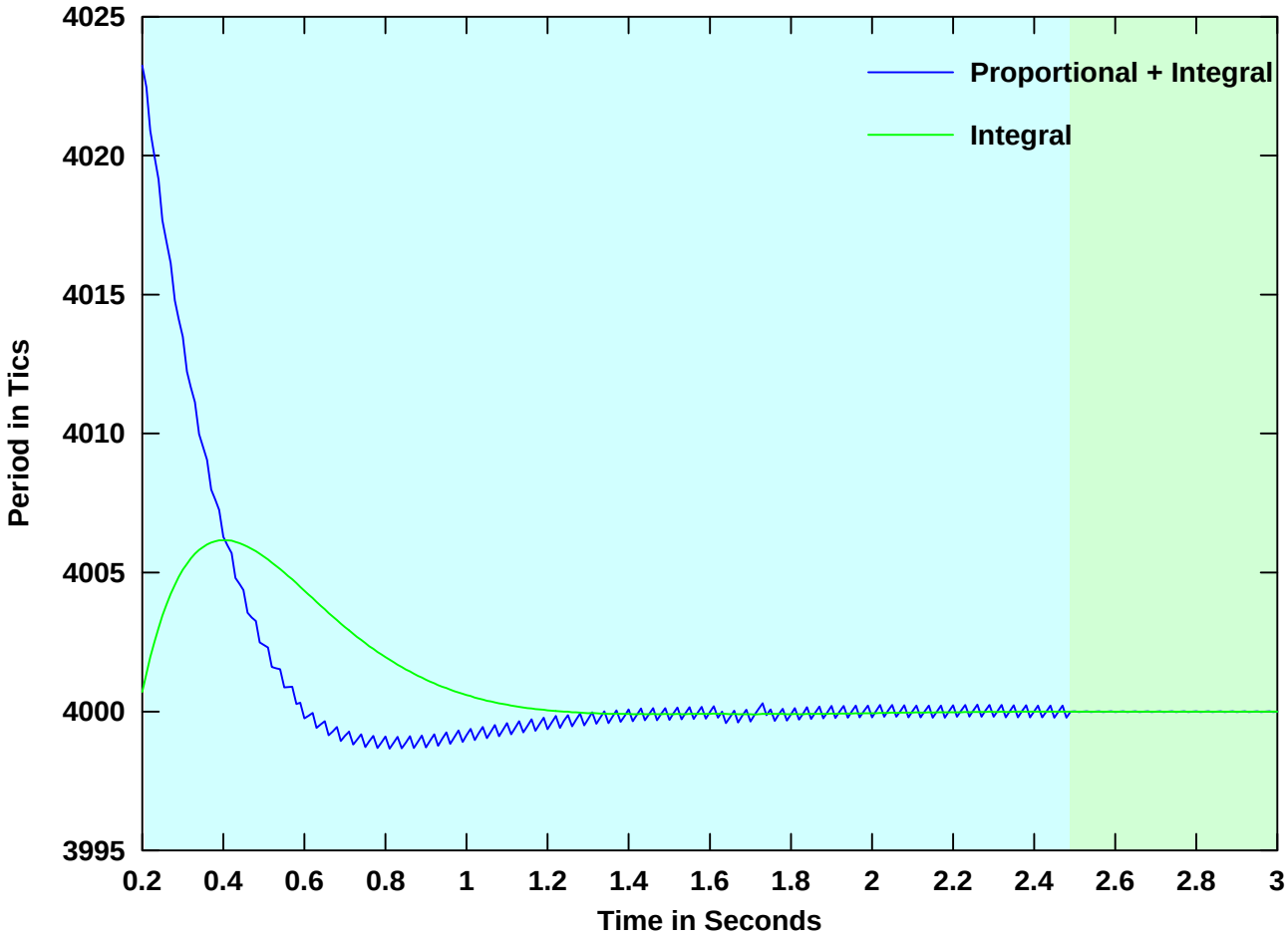
Phase Locked Loop Operation (1)



Phase Locked Loop Operation (2)



Phase Locked Loop Operation (3)



Phase Locked Loop Operation (4)