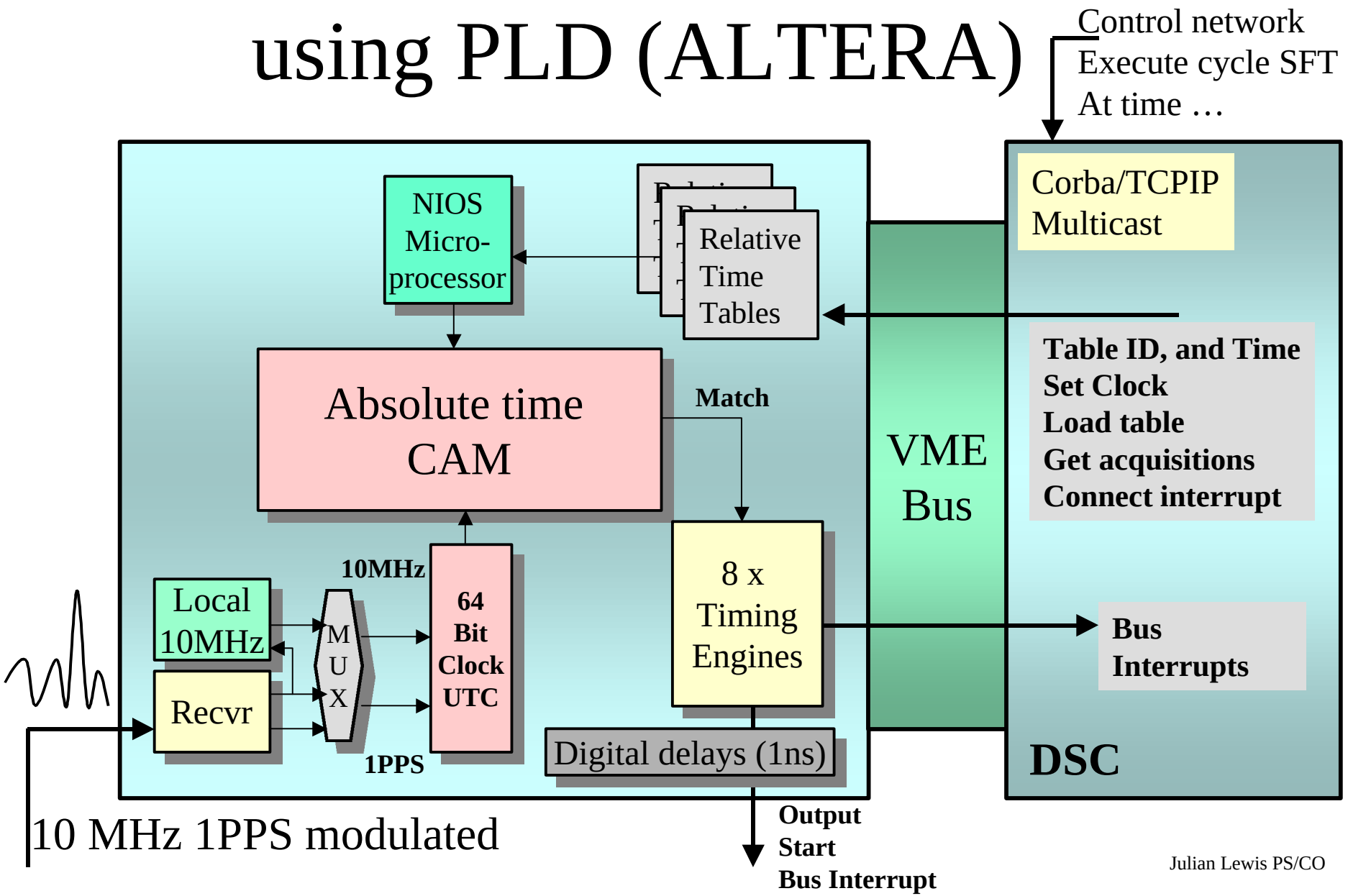
Future Timing Tg8 replacement using PLD (ALTERA)



Julian Lewis PS/CO

System Features

- Accepts table ID and 64 bit start time stamp.
- Relative time tables negative and positive values allow overlaps (forewarnings).
- Digital delay of 0.5 ns resolution. Jitter 1ns.
- Local high prescision10MHz source for stand alone / tests. Battery backup clock.
- Uses a reliable network protocol CORBA/TCPIP.
- Acquisitions available as time stamps.
- Bus interrupts for task scheduling.
- Autonomous operation, low control requirements.
- External clocks (100MHz), starts, chain, burst.
- All on one chip, reliable and cheap. In System Programmable (ISP)…