Transmission of B.S.T. messages using the TTC System.

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- The goal:

Transmission to all B.I. acquisition crates of:

> Timing Signals:
Bunch Clock (40 MHz)
Orbit Turn Clock (11 KHz)

> Beam Synchronous commands :
Injection Warnings.
Acquisition triggers.
Real time settings.
Post Mortem Synchronisation.

- The idea:

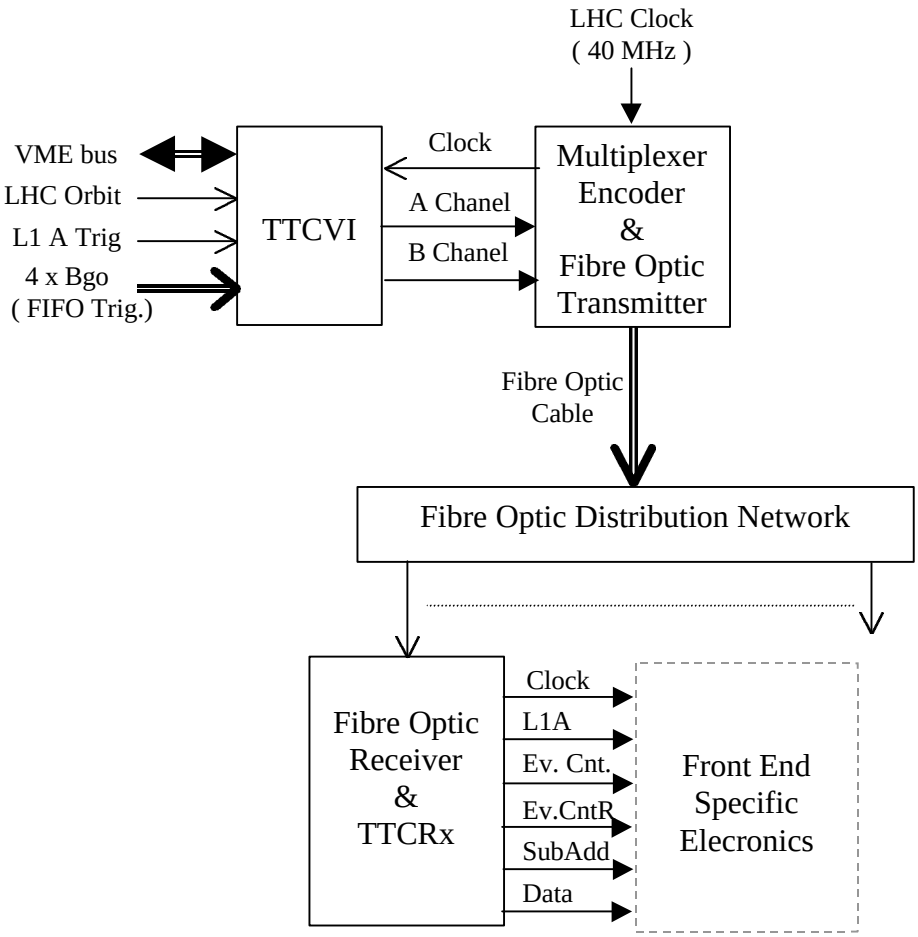
As well as using the TTC for the distribution of the 40MHz bunch clock and Orbit turn clock, we can profit from the TTC's ability to transmit additional data by inserting a BST message.

- Realisation:

Use as many TTC components as possible.

- …. Possible extension to Slow timing distribution.

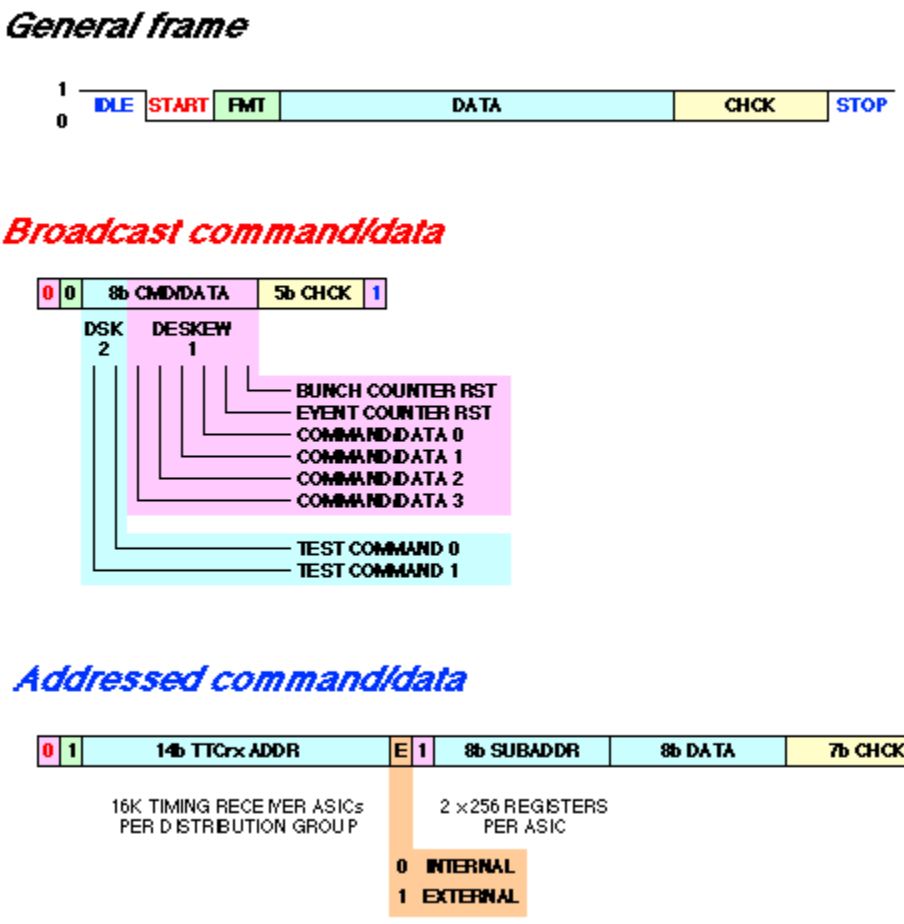
TTC system block diagram:



System features:

- Periodic transmission of commands from PCR to control crates.
- Broadcast or individual addressing mode.
- BST Message may contain up to 32 commands.
- Message transmission period: 88.924 μs. (LHC orbit period).
- Use of A channel (L1A trig.) to transmit LHC turn clock (Orbit Signal).
- Use of B channel to transmit BST message.
- Message data is alternately pre-loaded in 2 TTCvi FIFOs.
- The timing of the transmission relative to the orbit signal is controlled.
- Possible use of individually addressed commands for Reset or Test.
- Use of orbit counting facility.

TTC Frame description:

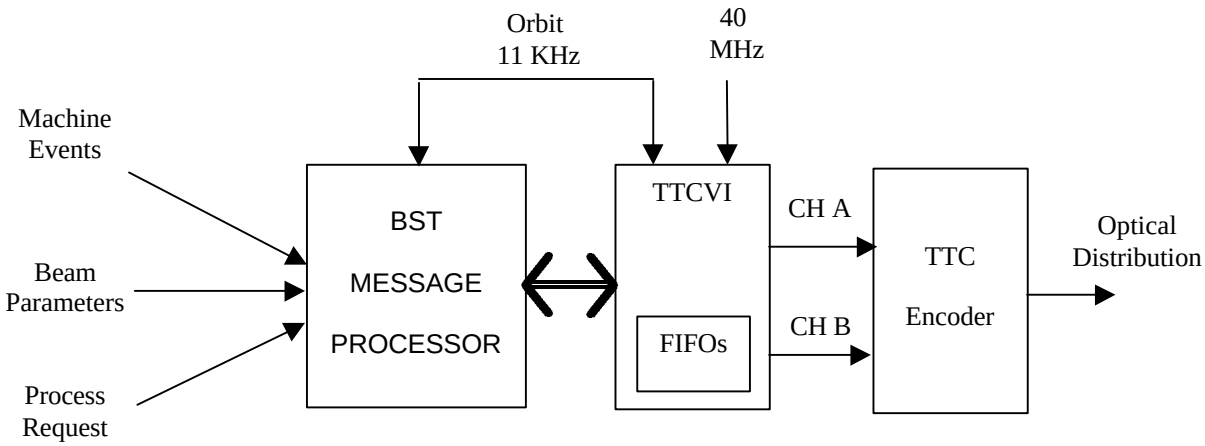


- If TTCrx ADDR = 0 : the command is broadcast to all TTCrx chips.
- A command with E bit = 0 (Internal), can be used to initialise TTCrx registers.
- 8 bit SubAddress allows the transmission of 256 *(32)* bytes of data.
- The maximum number of commands we can send within 88.9µs is 70 *(32)*.
- The FIFO's depth is 256 *(32)*, for a short or long format command.

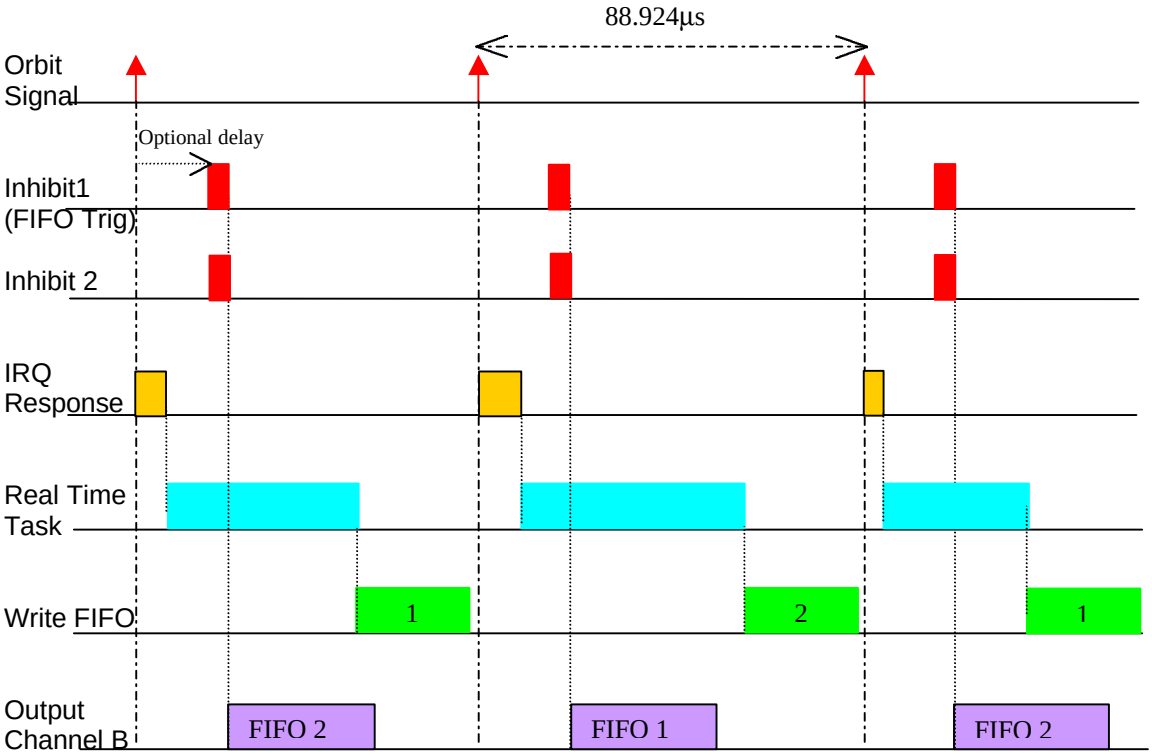
(BST needs)

Message Transmission:

Transmitter Bloc Diagram:



Transmission sequence:



! Maximum absolute values: IRQ Response + Real Time Task + Write FIFO < 88.9µs

IRQ Response :

Not predictable with an operating systems like LynxOS, it can be up to 30µs! But, we can modify the IRQ response routine, to fix this time to < 5 µs.

FIFO write:

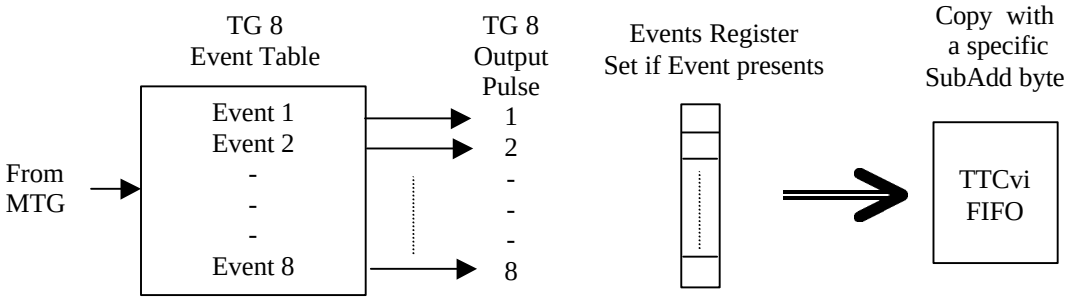
VME transfer takes 1 µs / longword on a PowerPC ⇒ 32µs for 32 commands. But, this can be reduced to 10µs in block transfer mode.

Real -Time Task:

A BST task consists of, for each instrument type, elabore the curent message.

A BST task can be synchronised with a GMT Event with TG8 module.

TG8 module can be used to pass on events using an Event table.



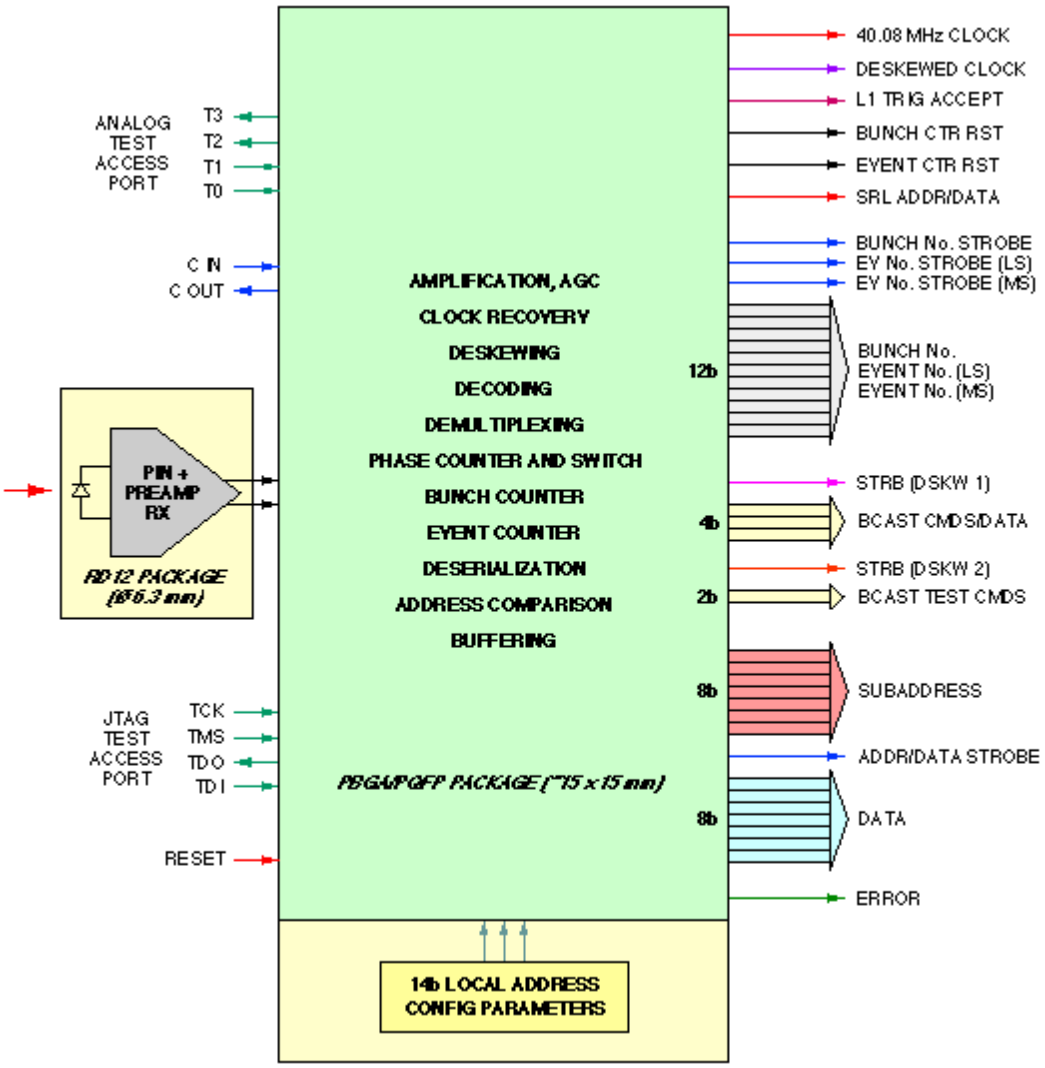
!! Limited to 8 Events (or 16 with 2 X TG8): OK to cover BI Needs !

The maximum time to execute the real time task is ~73µs for 32 commands !

Can be done with a PowerPC, but we need a faster processor.

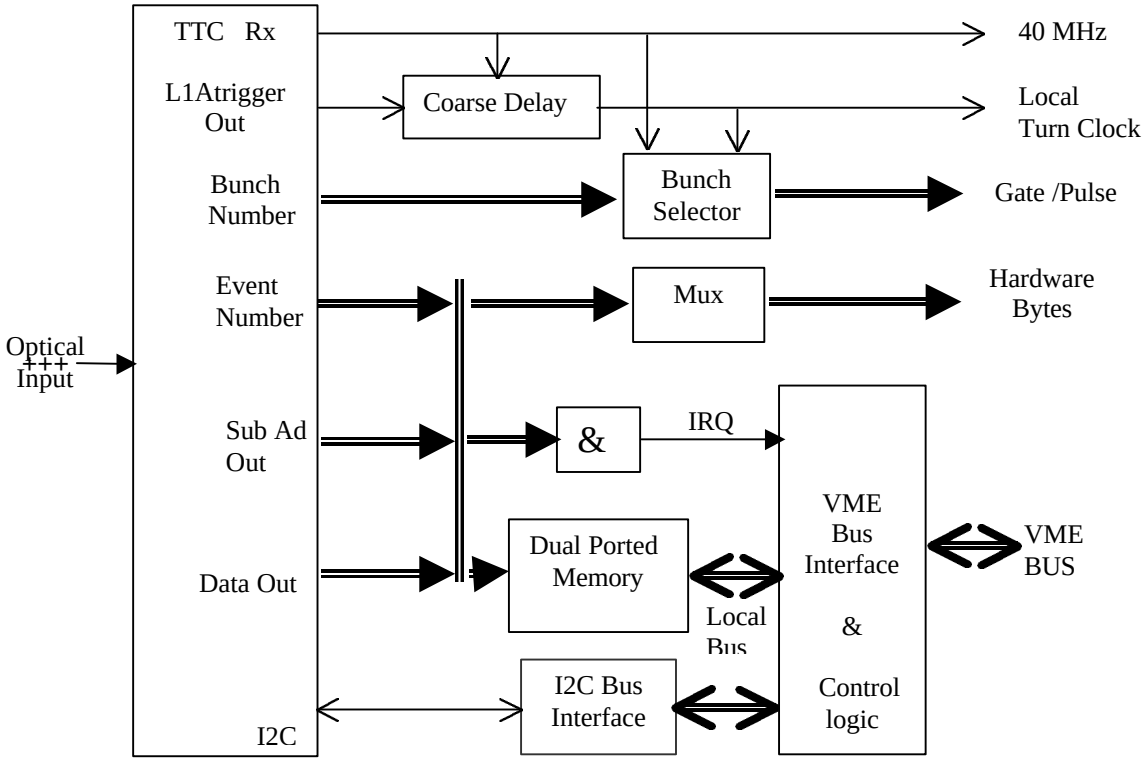
Increase the number of commands ⇒ Decrease the time for real-time task.

Message reception is based on the TTC Rx Chip:



Many functions are foreseen in the ASIC chip !

BST Receiver bloc diagram:



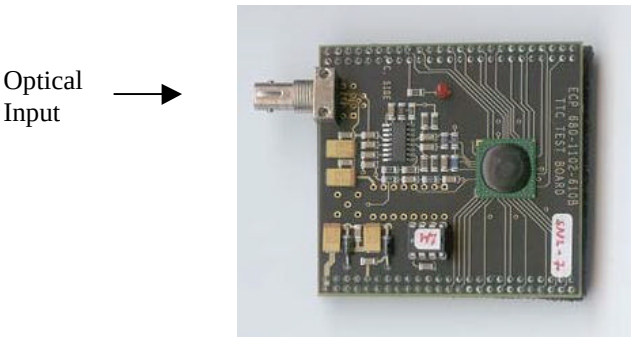
Additional features required to cover BI needs:

- Turn clock delay variable up to 88.924μs - current TTCRx chip only has a 0 to 375ns coarse delay range.
- Bunch Selector to provide 16 individual gates or pulses at any of the 3564 slots (25ns steps)
- So-called "hardware" bytes in the received message are sent directly to a hardware output.
- An 8 byte sub-address mask is used to allow a local interruption.
- All received messages are stored in dual ported memory which is updated every 88.924 μs.
- A VME - I2C bus interface allows the control all TTC Rx internal registers.
- All logic can be implemented in an FPGA and reprogrammed according to the application's needs.

2 possible implementations:

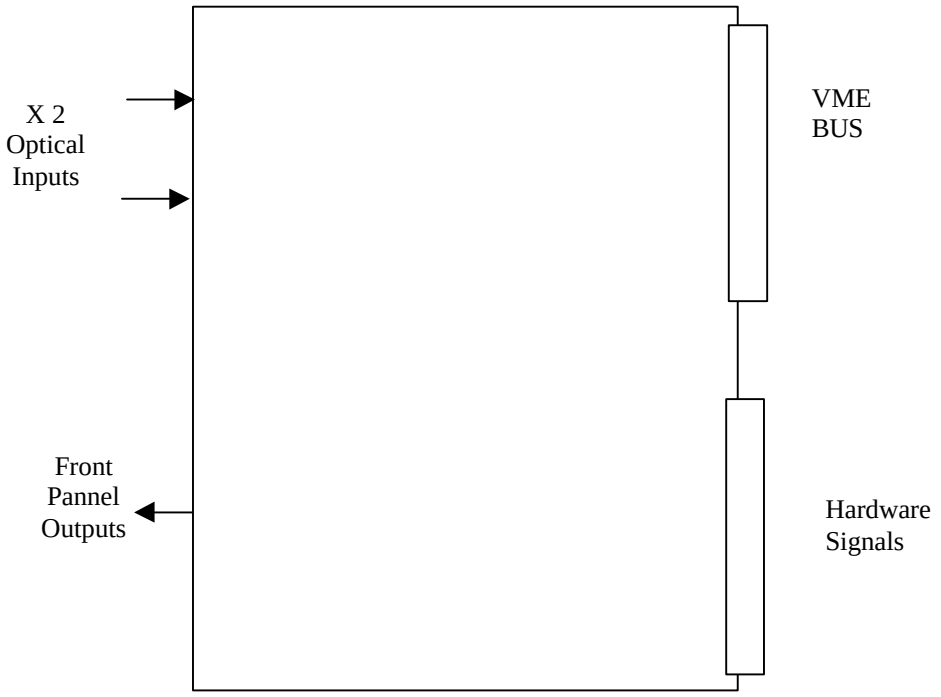
"Stand alone Version"

TTCRX Mezzanine board and FPGA put directly on the acquisition card.



"General purpose version "

VME board with all possible options and 2 identical parts, one for each ring.



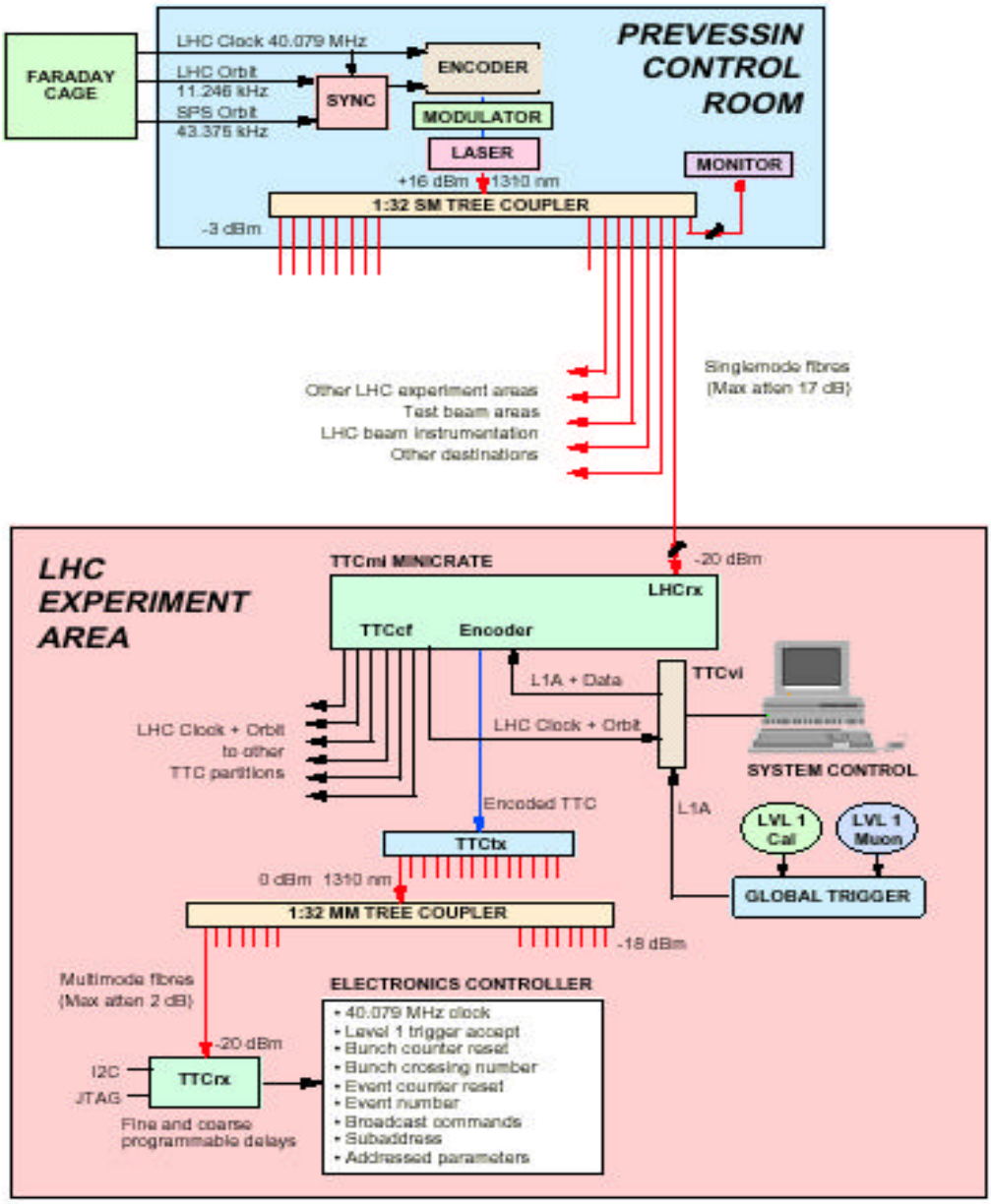
System architecture:

The overall TTC system architecture provides the distribution of synchronous timing signals from PCR to LHC Experiment Areas.

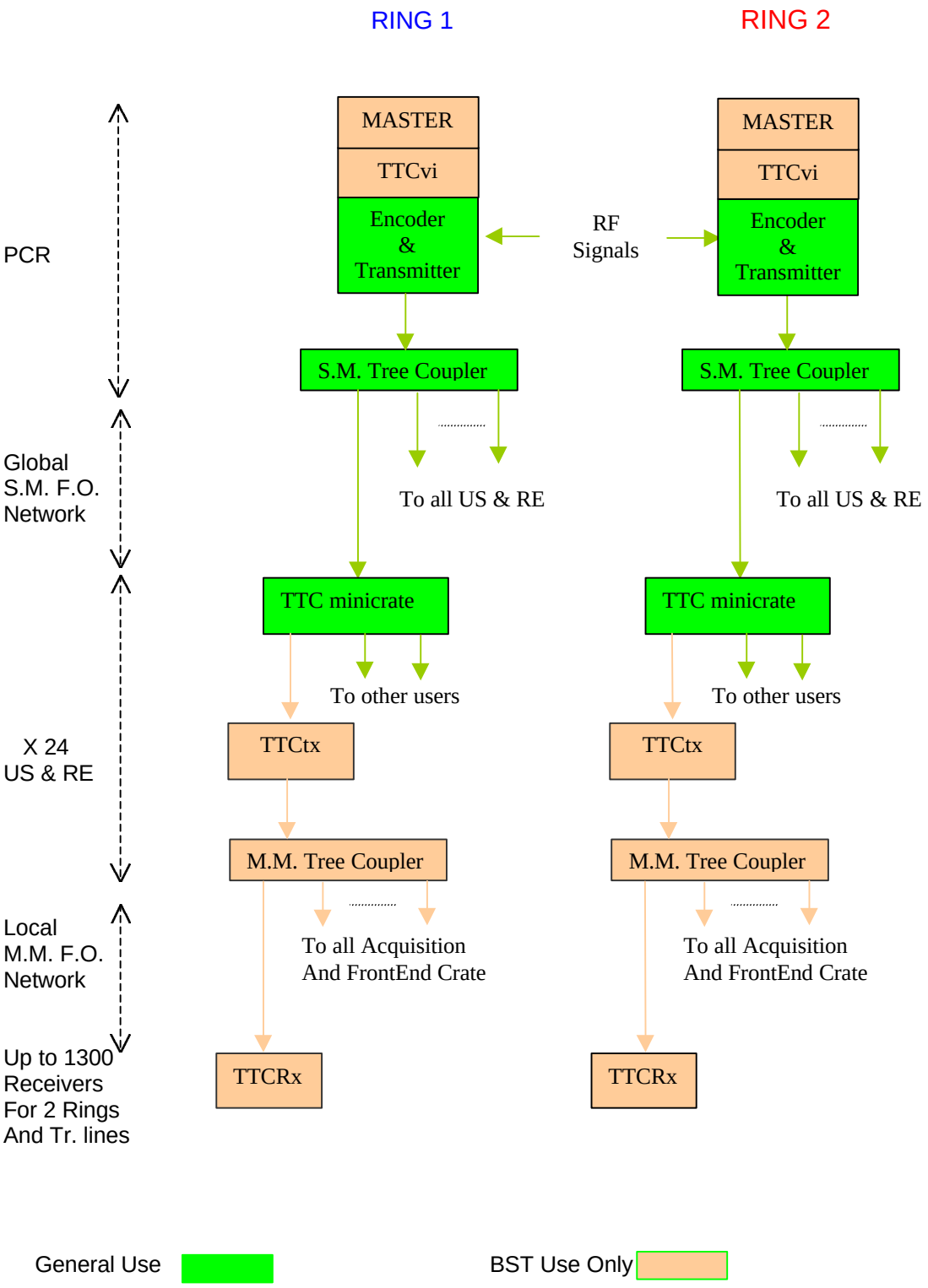
For BST message distribution, this network can be expanded to all LHC beam instrumentation control crates.

The local distribution and tunnel distribution (if required), can be done with a TTCtx module, as in the experiments.

Bloc Diagram of TTC distribution



Overall Topology



Possible extension to Slow timing distribution.

- Reserve some sub-addresses for slow timing events.
- At a periodic T ms tick from GPS, the Master writes the event to send to the TTCvi FIFO.
- At the next Orbit clock the FIFO contents are broadcast to all TTCRx.
- The propagation delay from the master to any TTCRx is less than 200µs.
- At time T + Propagation delay + 0…88.9µs, Events are stored in a buffer.
- At T + 1 ms tick from GPS, the Buffer is Read.